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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,488	03/07/2004	CHENG-HENG KAO	12476-US-PA	2487

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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
BEVERIDGE, RACHEL E	
ART UNIT	PAPER NUMBER
1725	

DATE MAILED: 03/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/708,488	KAO ET AL.	
	Examiner	Art Unit	
	Rachel E. Beveridge	1725	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-10,14-18,21-23,27 and 28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5, 7-10, 14-18, 21-23, and 27-28* is/are rejected.

7)☒ Claim(s) *16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to because figure 2B has the label "Cn" representing the copper layer. The examiner suggests changing this label to --Cu.-- Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: "For example, the copper layer, the nickel layer and the tin layer have thickness 4μm, 2μm,

3.2μm, 2.13μm respectively" (page 11, [0033], lines 3-5). The sentence lists three layers and four thickness; therefore, it is unclear which thickness concerns each layer. The examiner recognizes that the applicant discloses a gold layer (p. 11, [0033], line 2) and interpreted the 2.13μm disclosure to concern this layer.

Appropriate correction is required.

Claim Objections

Claim 16 is objected to because of the following informalities: Claim 16 recites the limitation "the % weight ratio" in line 3. There is insufficient antecedent basis for this limitation in the claim. The examiner suggests changing "the" to --a.-- Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 7-9, 16-18, and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davis et al. (US 5,280,414) in view of Ivey et al. (US 6,797,409 B2).

Davis teaches transient liquid bonding one metal, "such as gold, is deposited on a land, e.g. lands 35 and 45 and another metal, such as tin, is deposited on the corresponding land, e.g. lands 65 and 75, with which it is to be connected" (Davis et al.,

col. 3, lines 46-52). Davis discloses the metal coated lands (35,45,65,75) contacted and heated to a melting temperature that is slightly above the binary eutectic solder composition (col. 3, lines 53-57). See figure 11. Davis further discloses that a non-eutectic solder alloy composition resulting upon solidification will remain solid throughout subsequent dielectric processing temperatures and throughout the composite in the event a semiconductor chip (100) is solder mounted via the solder "bulls" (110) (col. 3, lines 57-65). Davis discloses that AuSn alloy with greater than about 20wt.% tin tends to be brittle; therefore, the ratio of Au/Sn should be "at least equal to about 1.5" (col. 5, lines 14-16). Furthermore, Davis teaches "AuSn20wt.% eutectic melts at about 280 degrees C; by reacting it with Au the melting point is raised to above about 490 degrees C; the resulting composition has the ductility and strength required to maintain joint integrity even when reheated to high performance polymer laminating temperatures (col. 5, lines 16-21). See the AuSn phase diagram disclosed in Davis's figure 1. Davis discloses the eutectic reaction at 287 degrees C (col. 6, line1) is AuSn + beta (Au_5Sn) → L at 280 degrees C (col. 6, lines 8-9). This therefore suggests a eutectic structure at temperatures in excess of 280°C. Davis further states that "after the Au-20wt%Sn eutectic is formed, it may react with the Au underneath further to form either beta phase or an AuSn solid solution before it melts" and the reaction was characterized by samples taken from heating rates from 3 to 100 degrees C/min. and measured at 280 degrees C (col. 6, lines 42-47). Also, Davis studied the reaction between the eutectic and Au at 295 and 390 degrees C (col. 6, lines 63-67 and col. 7, lines 1-2). Davis shows a SEM photo of a sample where the Au20wt%Sn eutectic

partially reacted with Au in figure 6 (col. 7, lines 18-19). Davis states, "the contrast used to reveal the layers in the Au-Sn section made the Cu foil invisible in the mircrograph" and that "three distinct layers can be seen in FIG. 6" where the layer on the right is unreacted Au (col. 7, lines 23-26). Davis analyzed the structure and discloses that the layer on the left (still in figure 6) had a composition close to 80 wt.% Au, which confirmed that the unreacted liquid AuSn remained at the eutectic composition (col. 7, lines 30-33). The middle layer was found to have a composition close to that of beta phase; therefore, Davis concluded that above the eutectic melting point, AuSn eutectic reacted with Au to form beta phase Au_5Sn (col. 7, lines 33-39). Figure 5A shows the layered structure of Au and Sn before heating and formation of the AuSn eutectic composition and thus meets the claim limitation for applying Sn over Au or applying Au over Sn, as that "over" can mean many things and does not limit the claim language to exclude Davis's disclosure. Although Davis suggests a eutectic structure at temperatures in excess of 280°C, Davis does not explicitly state this occurrence. Ivey discloses gold-tin (Au-Sn) eutectic solders "commonly used in the optoelectronic and microelectronic industries for chip bonding to dies" (Ivey et al., col. 1, lines 13-15). Ivey further states that "presently, most eutectic gold-tin alloys are prepared as solder performs" (col. 10, lines 40-41). Ivey discloses Au-Sn solder layers produced by "sequentially" depositing Au first on a seed layer then Sn (col. 1, lines 28-29). Ivey's disclosure includes applying the alloys in layers on one member. See column 5, lines 64-67 and column 6, lines 1-6. Ivey teaches that "it can be readily seen that a combination of Au_5Sn and AuSn ca readily produce a layered composite material which

has a composite material composition comprising anywhere between 15 at % tin and 50 at %tin, thus including the eutectic composition as well as near-eutectic compositions" (col. 6, lines 51-54). Furthermore, Ivey teaches that within the gold-tin alloy system, the first alloy species consists primarily of a first alloy phase Au_5Sn and the second alloy species consists primarily of a second alloy phase AuSn (col. 6, lines 64-68). Ivey also states that by further minimizing the thickness of the layers comprising the layered composite material, a "completely interspersed structure can be approximated which will exhibit essentially the same physical properties as an equivalent alloy composition which does possess a true interspersed structure" (col. 11, lines 35-39). Ivey shows SEM micrographs of deposits obtained in figure 8 (col. 20, lines 41-42). Ivey discloses that the fine microstructure obtained may be due in part to its high Au content or low Sn content of 16.7% (col. 20, lines 44-45). Furthermore, Ivey discloses an electrodeposition process for producing a layered composite material and the layered composite material produced by the process (abstract, lines 1-2). Ivey states that the process includes the steps of energizing an electroplating circuit to provide a current to deposit a layer of the first alloy species and next energizing another electroplating circuit to provide a current to deposit a layer of the second alloy species (abstract, lines 7-11). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the invention of Davis to include the eutectic structure formed by Ivey's electrodeposition and bonding method in order to utilize a hard solder well suited for long term reliability of the packaging application (Ivey et al., col. 10, lines 32-39).

Claims 10 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davis et al. (US 5,280,414) and Ivey et al. (US 6,797,409 B2) as applied to claim 1 above, and further in view of Coult et al. (US 5,90,560).

With respect to claim 10, Davis and Ivey lack disclosure of forming an adhesion layer, barrier layer, and wetting layer on one or both of the two members for bonding before forming the tin layer and the gold layer. Coult discloses a solder layer (12), comprised of three layers (12a,12b,12c), a quenching layer (14), a control layer (16), and the two parts (30,32) to be bonded together (Coult et al., col. 6, lines 4-8). Coult further discloses a barrier layer (18) disposed on the surface of the solder layer (12) or between the solder layer (12) and control layer (16) (col. 6, lines 8-11). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined invention of Davis and Ivey to include the wetting, barrier, and solder (adhesion) layers of Coult in order to prohibit the undesired oxidation of the solder or oxidizable components of the solder (Coult et al., col. 6, lines 11-19).

With respect to claim 15, Davis and Ivey lack disclosure of a photo-electronic device for bonding to a substrate. Coult directs his invention to optical subassemblies and gold-tin solders (Coult et al., col. 4, lines 25-28). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined invention of Davis and Ivey to include the optical electronics of Coult in order to form improved bonds between the optical devices and the substrate, where the bonds remain solid at temperatures above the melting point of the original solder composition and improve the control of the solder materials (Coult, col. 3, lines 21-26).

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Davis et al. (US 5,280,414) and Ivey et al. (US 6,797,409 B2) as applied to claim 1 above, and further in view of Kajiwara et al. (US 2002/0056906 A1).

Davis and Ivey lack specific disclosure of a flip-chip for bonding to a substrate. Kajiwara discloses a flip chip assembly (Kajiwara, p.4, [0056], lines 1-5) where one solder bump of semi-cured resin is formed on the PCB substrate and the other formed on the semiconductor chip (p.4, [0056], lines 8-12). Kajiwara further discloses heating the assembly so that the bumps are metallically joined to each other, and teaches the bumps to be made of a precious metal, for example Au (p.4, [0056], lines 12-17). Kajiwara discloses continuously heating until the work temperature exceeds the Au-Sn eutectic temperature (p.9, [0097], lines 17-19). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined invention of Davis and Ivey to include the flip chip disclosure of Kajiwara in order to reduce the electrical resistance of the connection part, enhance the reliability of the assembly, and minimize the structural size of the small semiconductor package (Kajiwara et al., p.10, [0100], lines 1-11).

Claims 23 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davis et al. (US 5,280,414) and Ivey et al. (US 6,797,409 B2) as applied to claim 16 above, and further in view of Coult et al. (US 5,90,560).

With respect to claim 23, Davis and Ivey lack disclosure of forming an adhesion layer, barrier layer, and wetting layer on one or both of the two members for bonding before forming the tin layer and the gold layer. Coult discloses a solder layer (12), comprised of three layers (12a,12b,12c), a quenching layer (14), a control layer (16), and the two parts (30,32) to be bonded together (Coult et al., col. 6, lines 4-8). Coult further discloses a barrier layer (18) disposed on the surface of the solder layer (12) or between the solder layer (12) and control layer (16) (col. 6, lines 8-11). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined invention of Davis and Ivey to include the wetting, barrier, and solder (adhesion) layers of Coult in order to prohibit the undesired oxidation of the solder or oxidizable components of the solder (Coult et al., col. 6, lines 11-19).

With respect to claim 28, Davis and Ivey lack disclosure of a photo-electronic device for bonding to a substrate. Coult directs his invention to optical subassemblies and gold-tin solders (Coult et al., col. 4, lines 25-28). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined invention of Davis and Ivey to include the optical electronics of Coult in order to form improved bonds between the optical devices and the substrate, where the bonds remain solid at temperatures above the melting point of the original solder composition and improve the control of the solder materials (Coult, col. 3, lines 21-26).

Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Davis et al. (US 5,280,414) and Ivey et al. (US 6,797,409 B2) as applied to claim 16 above, and further in view of Kajiwara et al. (US 2002/0056906 A1).

Davis and Ivey lack specific disclosure of a flip-chip for bonding to a substrate. Kajiwara discloses a flip chip assembly (Kajiwara, p.4, [0056], lines 1-5) where one solder bump of semi-cured resin is formed on the PCB substrate and the other formed on the semiconductor chip (p.4, [0056], lines 8-12). Kajiwara further discloses heating the assembly so that the bumps are metallically joined to each other, and teaches the bumps to be made of a precious metal, for example Au (p.4, [0056], lines 12-17). Kajiwara discloses continuously heating until the work temperature exceeds the Au-Sn eutectic temperature (p.9, [0097], lines 17-19). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined invention of Davis and Ivey to include the flip chip disclosure of Kajiwara in order to reduce the electrical resistance of the connection part, enhance the reliability of the assembly, and minimize the structural size of the small semiconductor package (Kajiwara et al., p.10, [0100], lines 1-11).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rachel E. Beveridge whose telephone number is 571-

272-5169. The examiner can normally be reached on Monday through Friday, 9 am to 6 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Ryan can be reached on 571-272-1292. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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JONATHAN JOHNSON
PRIMARY EXAMINER